ANALOG DEVICES

Low Power, Low Noise Precision FET Op Amp

AD795

FEATURES
Low Power Replacement for Burr-Brown OPA-111, OPA-121 Op Amps
Low Noise
- **2.5 µV p-p max, 0.1 Hz to 10 Hz**
- **11 nV/√Hz max at 10 kHz**
- **0.6 fA/√Hz at 1 kHz**

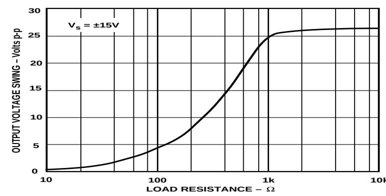
High DC Accuracy
- **250 µV max Offset Voltage**
- **3 µV/°C max Drift**
- **1 pA max Input Bias Current**
- **Low Power: 1.5 mA max Supply Current**

Available in Low Cost Plastic Mini-DIP and Surface Mount (SOIC) Packages

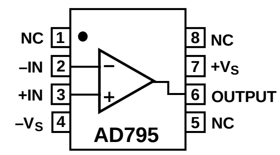
APPLICATIONS
Low Noise Photodiode Preamps
CT Scanners
Precision I-to-V Converters

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package



8-Pin SOIC (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

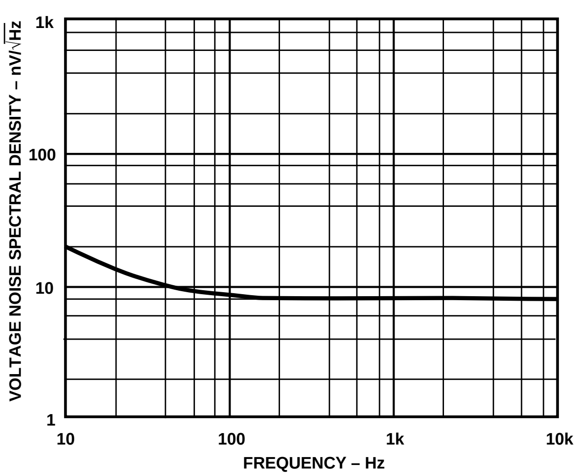
The AD795 is a low noise, precision, FET input operational amplifier. It offers both the low voltage noise and low offset drift of a bipolar input op amp and the very low bias current of a FET-input device. The 10^{14} Ω common-mode impedance insures that input bias current is essentially independent of common-mode voltage and supply voltage variations.

The AD795 has both excellent dc performance and a guaranteed and tested maximum input voltage noise. It features 1 pA maximum input bias current and 250 µV maximum offset voltage, along with low supply current of 1.5 mA max.

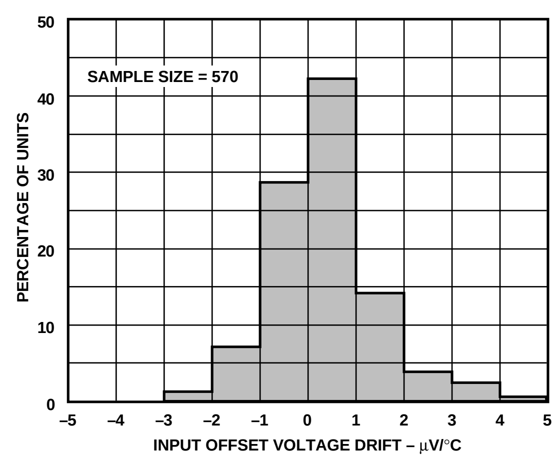
Furthermore, the AD795 features a guaranteed low input noise of 2.5 µV p-p (0.1 Hz to 10 Hz) and a 11 nV/√Hz max noise level at 10 kHz. The AD795 has a fully specified and tested input offset voltage drift of only 3 µV/°C max.

The AD795 is useful for many high input impedance, low noise applications. The AD795J and AD795K are rated over the commercial temperature range of 0°C to +70°C.

The AD795 is available in 8-pin plastic mini-DIP and 8-pin surface mount (SOIC) packages.



AD795 Voltage Noise Spectral Density



Typical Distribution of Average Input Offset Voltage Drift

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD795–SPECIFICATIONS (@ +25°C and ±15 V dc unless otherwise noted)

Parameter	Conditions	AD795JN/JR Min	AD795JN/JR Typ	AD795JN/JR Max	AD795K Min	AD795K Typ	AD795K Max	Units
INPUT OFFSET VOLTAGE[1]								
Initial Offset			100	500		50	250	µV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400	µV
vs. Temperature			3	10		1	3	µV/°C
vs. Supply (PSRR)		86	110		90	110		dB
vs. Supply (PSRR)	T_{MIN}–T_{MAX}	84	100		87	100		dB
INPUT BIAS CURRENT[2]								
Either Input	V_{CM} = 0 V		1	2/3		1	1	pA
Either Input @ T_{MAX} =	V_{CM} = 0 V		23			23		pA
Either Input	V_{CM} = +10 V		1			1		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.6	pA
Offset Current @ T_{MAX} =	V_{CM} = 0 V		2			2		pA
OPEN-LOOP GAIN	V_O = ±10 V							
	R_{LOAD} ≥ 10 kΩ	110	120		110	120		dB
	R_{LOAD} ≥ 10 kΩ	100	108		100	108		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		1.0	3.3		1.0	2.5	µV p-p
	f = 10 Hz		20	50		20	40	nV/√Hz
	f = 100 Hz		12	40		12	30	nV/√Hz
	f = 1 kHz		11	17		11	15	nV/√Hz
	f = 10 kHz		9	11		9	11	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 Hz to 10 Hz		13			13		fA p-p
	f = 1 kHz		0.6			0.6		fA/√Hz
FREQUENCY RESPONSE								
Unity Gain, Small Signal	G = –1		1.6			1.6		MHz
Full Power Response	V_O = 20 V p-p							
	R_{LOAD} = 2 kΩ		16			16		kHz
Slow Rate, Unity Gain	V_{OUT} = 20 V p-p							
	R_{LOAD} = 2 kΩ		1			1		V/µs
SETTLING TIME[3]								
To 0.1%	10 V Step		10			10		µs
To 0.01%	10 V Step		11			11		µs
Overload Recovery[4]	50% Overdrive		2			2		µs
Total Harmonic	f = 1 kHz							
Distortion	R1 ≥ 10 kΩ							
	V_O = 3 V rms		–108			–108		dB
INPUT IMPEDANCE								
Differential	V_{DIFF} = ±1 V		$10^{12}\|2$			$10^{12}\|2$		Ω‖pF
Common Mode			$10^{14}\|2.2$			$10^{14}\|2.2$		Ω‖pF
INPUT VOLTAGE RANGE								
Differential[5]			±20			±20		V
Common-Mode Voltage		±10	±11		±10	±11		V
Over Max Operating Temperature		±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		dB
	T_{MIN}–T_{MAX}	86	100		90	100		dB
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD} ≥ 2 kΩ	V_S –4	V_S –2.5		V_S –4	V_S –2.5		V
	T_{MIN}–T_{MAX}	V_S –4			V_S –4			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		mA
	Short Circuit		±15			±15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±4		±18	±4		±18	V
Quiescent Current			1.3	1.5		1.3	1.5	mA

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Gain = –1, R1 = 10 kΩ.
[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.
[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2] (@ T_A = +25°C)
  SOIC Package . . . . 500 mW
  8-Pin Mini-DIP Package . . . . 750 mW
Input Voltage . . . . $\pm V_S$
Output Short Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . $+V_S$ and $-V_S$
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range
  AD795J/K . . . . 0°C to +70°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Mini-DIP Package: θ_{JA} = 100°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD795 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD795JN	0°C to +70°C	N-8
AD795KN	0°C to +70°C	N-8
AD795JR	0°C to +70°C	R-8

*N = Plastic mini-DIP; R = SOIC package.

AD795–Typical Characteristics

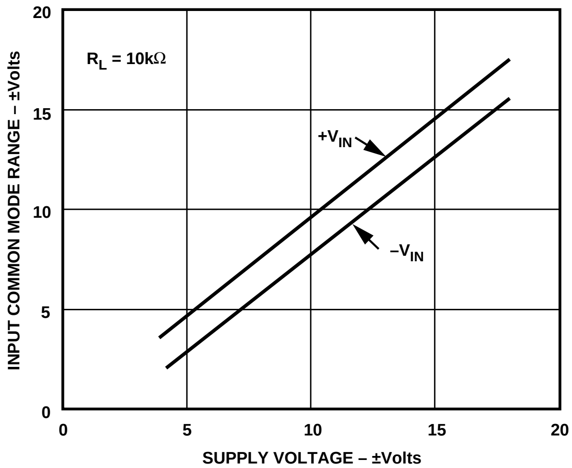


Figure 1. Common-Mode Voltage Range vs. Supply

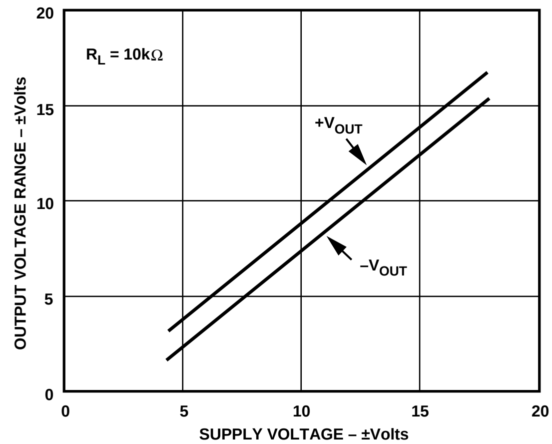


Figure 2. Output Voltage Range vs. Supply Voltage

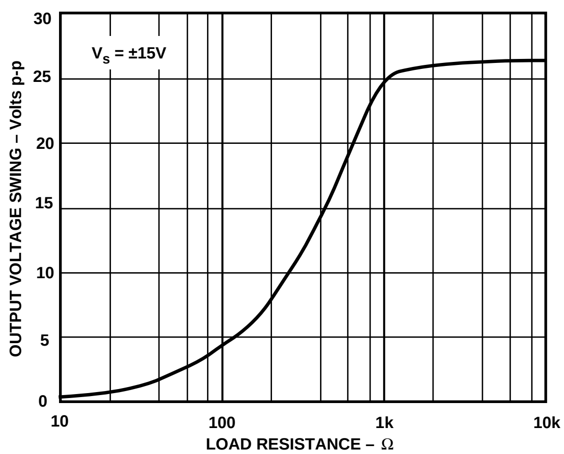


Figure 3. Output Voltage Swing vs. Load Resistance

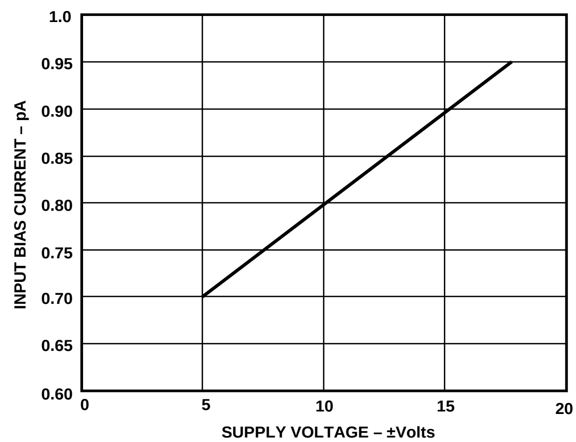


Figure 4. Input Bias Current vs. Supply

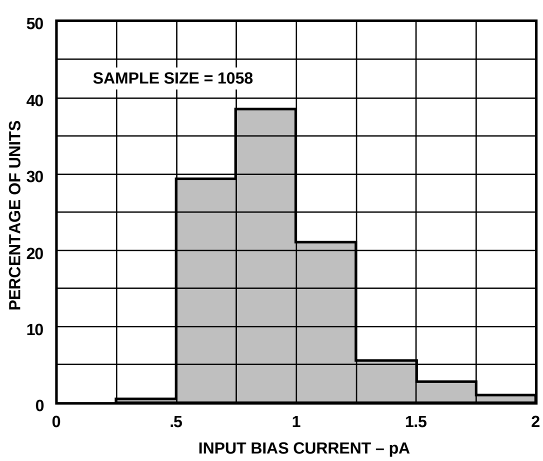


Figure 5. Typical Distribution of Input Bias Current

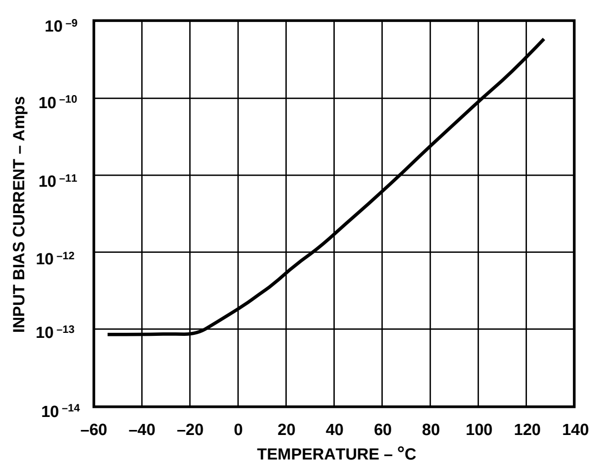


Figure 6. Input Bias Current vs. Temperature

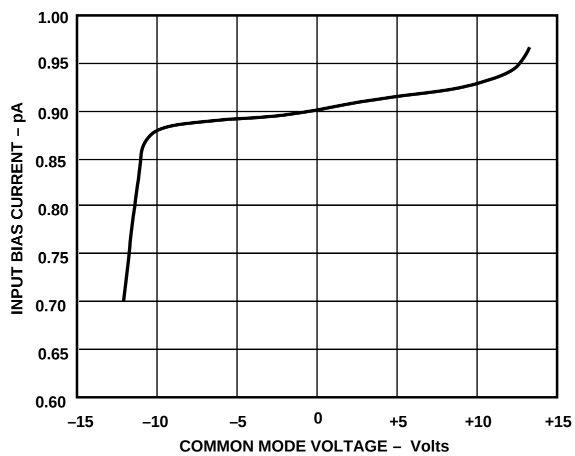


Figure 7. Input Bias Current vs. Common-Mode Voltage

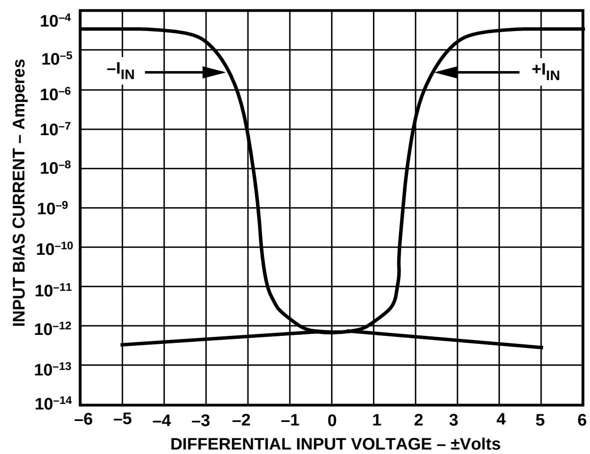


Figure 8. Input Bias Current vs. Differential Input Voltage

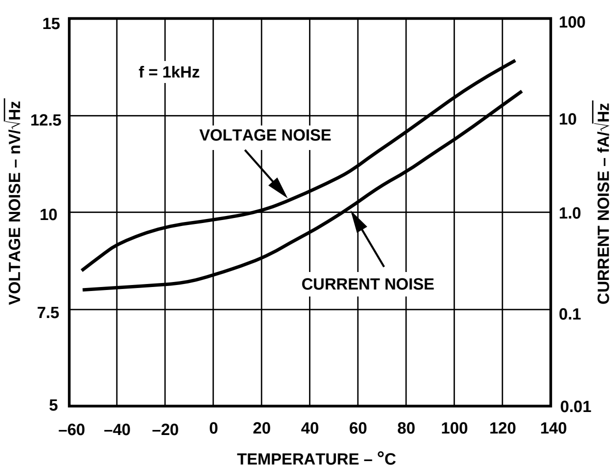


Figure 9. Voltage and Current Noise Spectral Density vs. Temperature

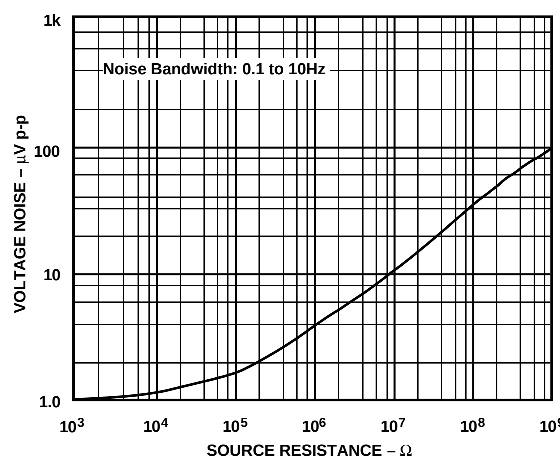


Figure 10. Input Voltage Noise vs. Source Resistance

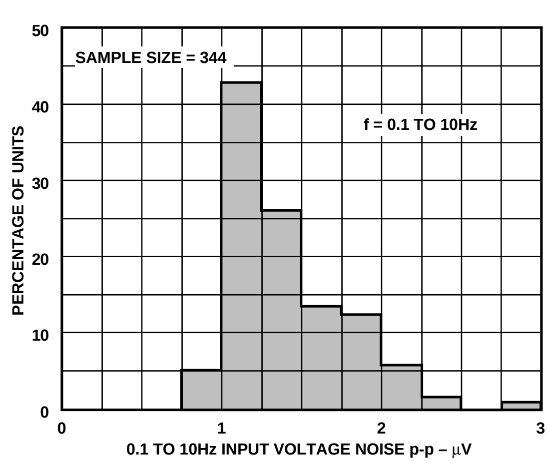


Figure 11. Typical Distribution of Input Voltage Noise

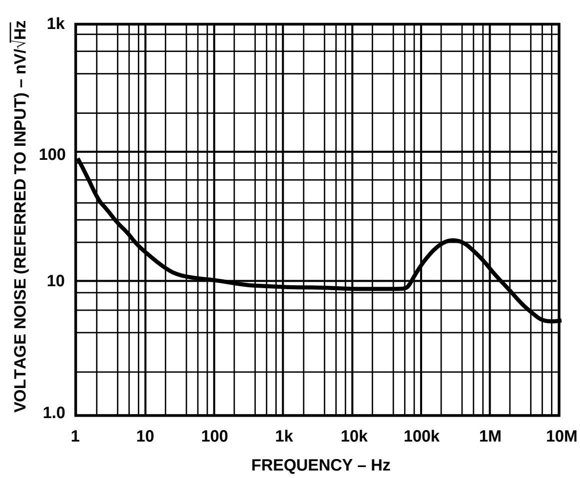


Figure 12. Input Voltage Noise Spectral Density

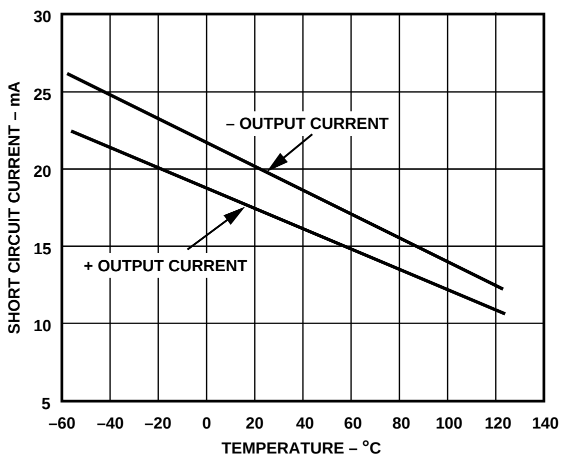


Figure 13. Short Circuit Current Limit vs. Temperature

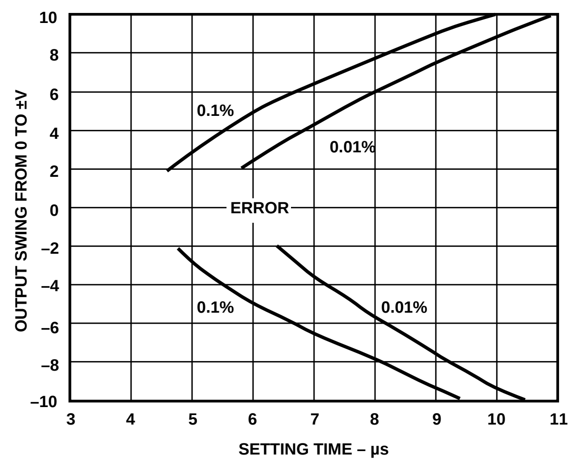


Figure 14. Output Swing and Error vs. Settling Time

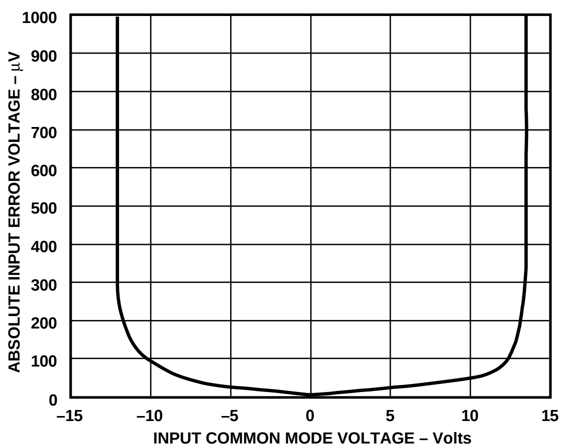


Figure 15. Absolute Input Error Voltage vs. Input Common-Mode Voltage

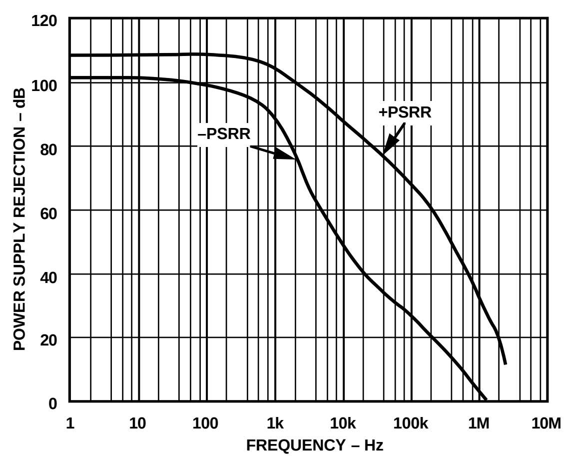


Figure 16. Power Supply Rejection vs. Frequency

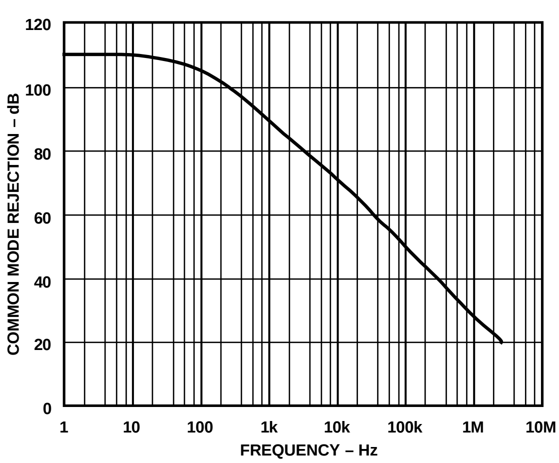


Figure 17. Common-Mode Rejection vs. Frequency

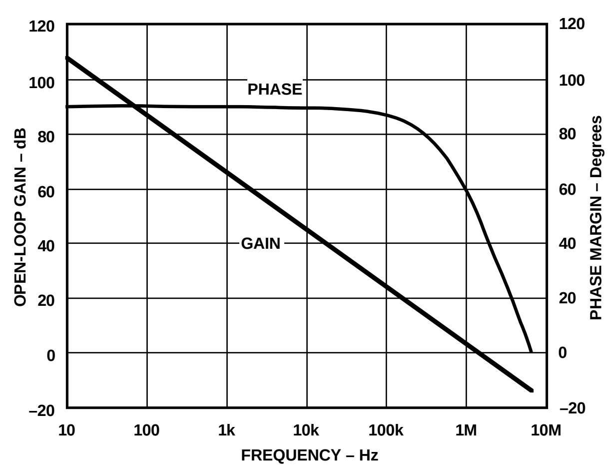


Figure 18. Open-Loop Gain & Phase Margin vs. Frequency

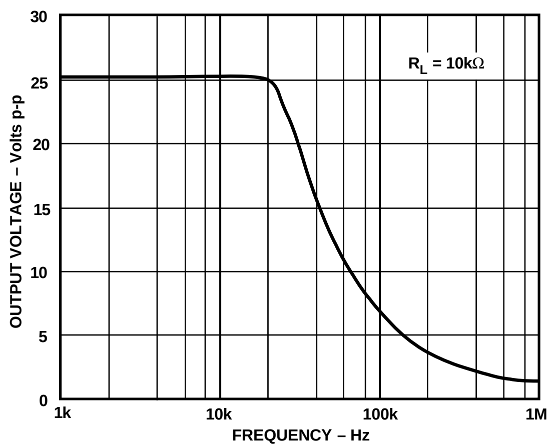


Figure 19. Large Signal Frequency Response

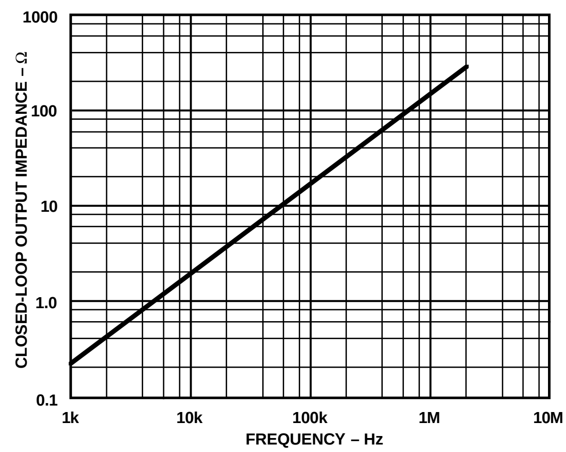


Figure 20. Closed-Loop Output Impedance vs. Frequency

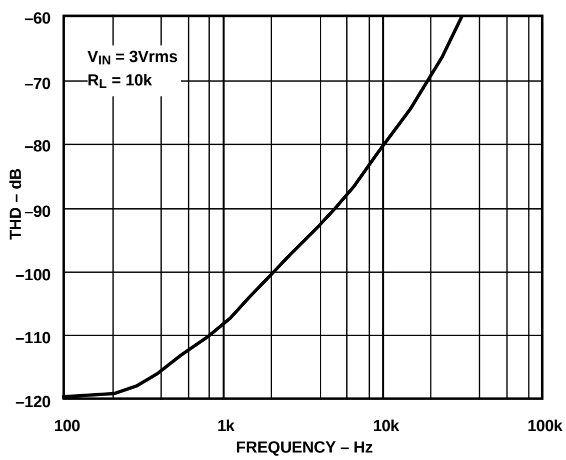


Figure 21. Total Harmonic Distortion vs. Frequency

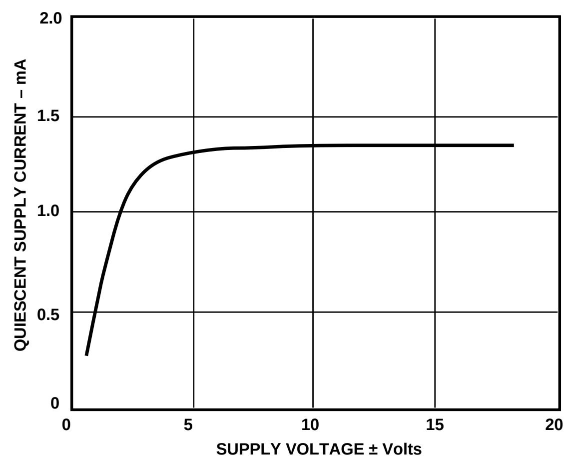


Figure 22. Quiescent Supply Current vs. Supply Voltage Drift

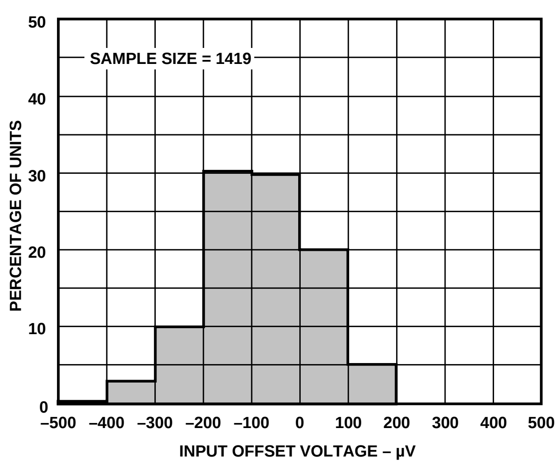


Figure 23. Typical Distribution of Input Offset Voltage

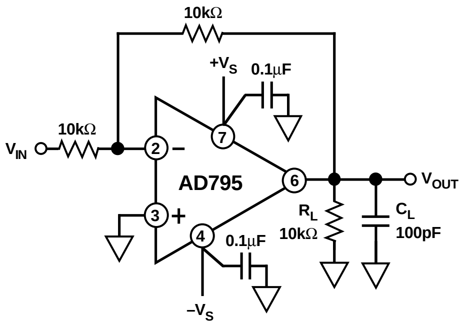


Figure 24. Unity Gain Inverter

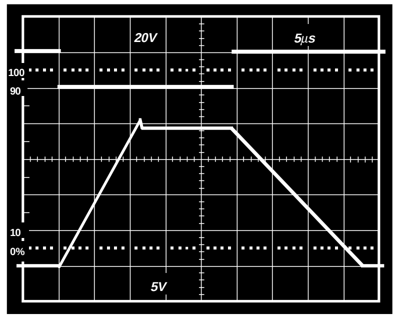


Figure 25. Unity Gain Inverter Large Signal Pulse Response

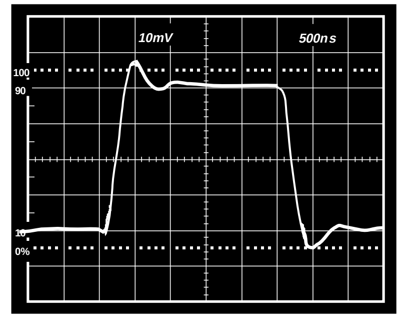


Figure 26. Unity Gain Inverter Small Signal Pulse Response

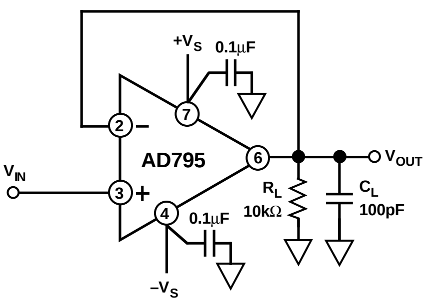


Figure 27. Unity Gain Follower

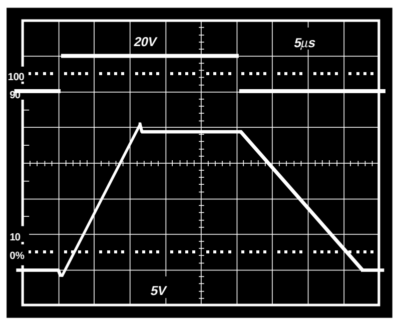


Figure 28. Unity Gain Follower Large Signal Pulse Response

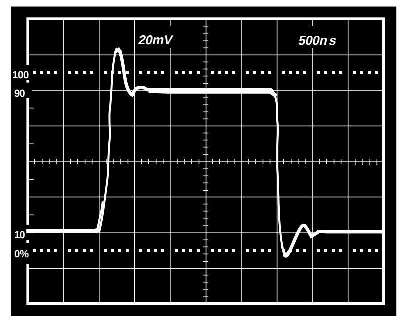


Figure 29. Unity Gain Follower Small Signal Pulse Response

MINIMIZING INPUT CURRENT

The AD795 is guaranteed to 1 pA max input current with ±15 volt supply voltage at room temperature. Careful attention to how the amplifier is used will maintain or possibly better this performance.

The amplifier's operating temperature should be kept as low as possible. Like other JFET input amplifier's, the AD795's input current will double for every 10°C rise in junction temperature (illustrated in Figure 6). On-chip power dissipation will raise the device operating temperature, causing an increase in input current. Reducing supply voltage to cut power dissipation will reduce the AD795's input current (Figure 4). Heavy output loads can also increase chip temperature, maintaining a minimum load resistance of 10 kΩ is recommended.

CIRCUIT BOARD NOTES

The AD795 is designed for throughhole mounting on PC boards, using either mini-DIP or surface mount (SOIC). Maintaining picoampere resolution in those environments requires a lot of care. Both the board and the amplifier's package have finite resistance. Voltage differences between the input pins and other pins as well as PC board metal traces will cause parasitic currents (Figure 30) larger than the AD795's input current unless special precautions are taken. Two methods of minimizing parasitic leakages are guarding of the input lines and maintaining adequate insulation resistance.

Figures 31 and 32 show the recommended guarding schemes for follower and inverted topologies. Note that for the mini-DIP, the guard trace should be on both sides of the board. On the SOIC, Pin 1 is not connected, and can be safely connected to the guard. The high impedance input trace should be guarded on both edges for its entire length.

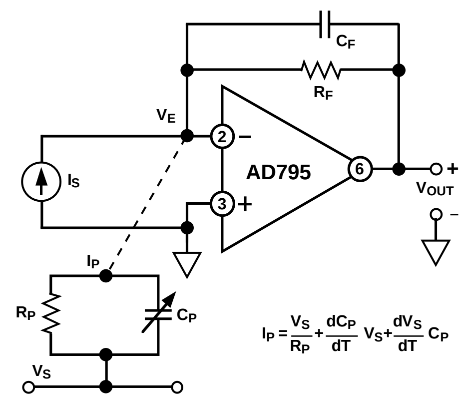


Figure 30. Sources of Parasitic Leakage Currents

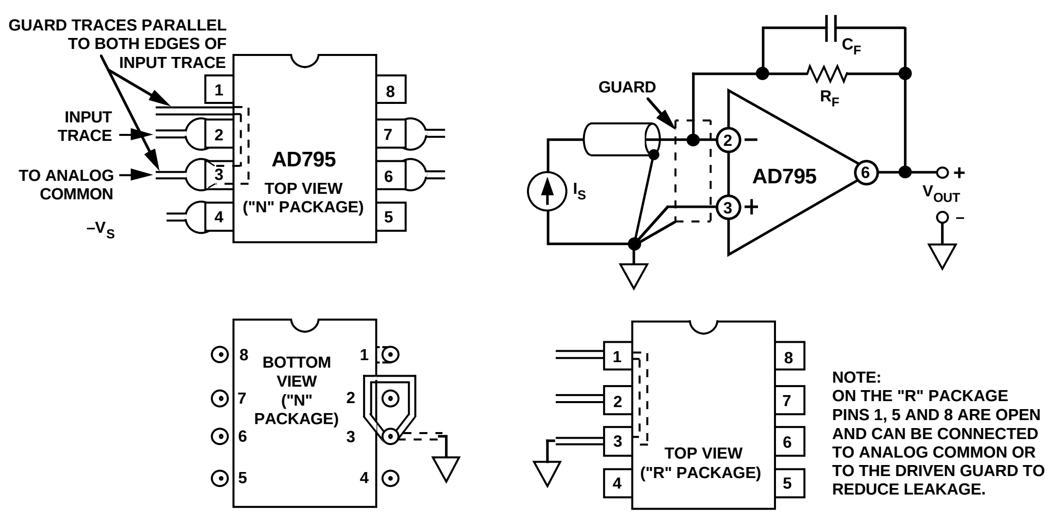


Figure 31. Guarding Scheme–Inverter

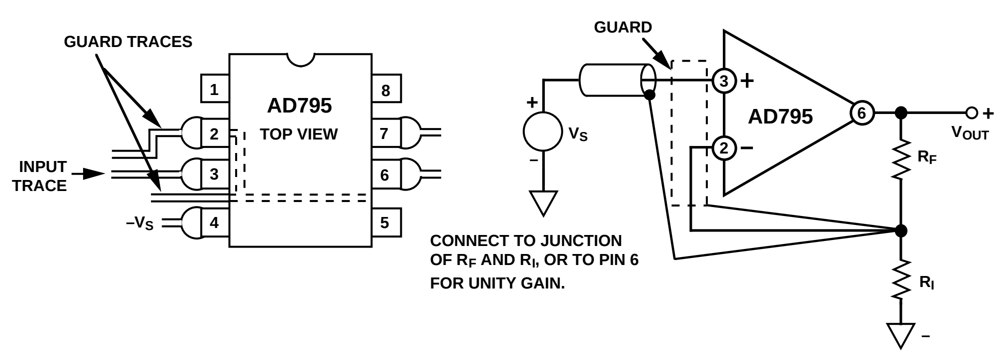


Figure 32. Guard Scheme–Follower

Leakage through the bulk of the circuit board will still occur with the guarding schemes shown in Figures 31 and 32. Standard "G10" type printed circuit board material may not have high enough volume resistivity to hold leakages at the subpicoampere level particularly under high humidity conditions. One option that eliminates all effects of board resistance is shown in Figure 33. The AD795's sensitive input pin (either Pin 2 when connected as an inverter, or Pin 3 when connected as a follower) is bent up and soldered directly to a Teflon* insulated standoff. Both the signal input and feedback component leads must also be insulated from the circuit board by Teflon standoffs or low-leakage shielded cable.

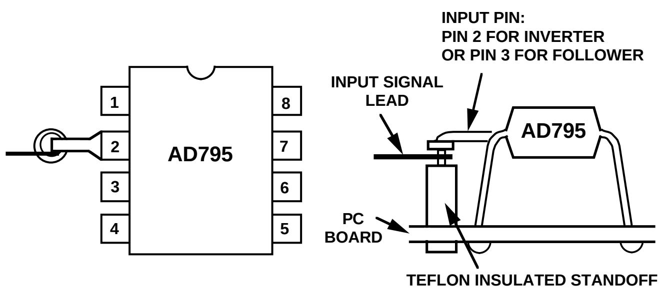


Figure 33. Input Pin to Insulating Standoff

Contaminants such as solder flux on the board's surface and on the amplifier's package can greatly reduce the insulation resistance between the input pin and those traces with supply or signal voltages. Both the package and the board must be kept clean and dry. An effective cleaning procedure is to first swab the surface with high grade isopropyl alcohol, then rinse it with deionized water and, finally, bake it at 100°C for 1 hour. Polypropylene and polystyrene capacitors should not be subjected to the 100°C bake as they will be damaged at temperatures greater than 80°C.

Other guidelines include making the circuit layout as compact as possible and reducing the length of input lines. Keeping circuit board components rigid and minimizing vibration will reduce triboelectric and piezoelectric effects. All precision high impedance circuitry requires shielding from electrical noise and interference. For example, a ground plane should be used under all high value (i.e., greater than 1 MΩ) feedback resistors. In some cases, a shield placed over the resistors, or even the entire amplifier, may be needed to minimize electrical interference originating from other circuits. Referring to the equation in Figure 30, this coupling can take place in either, or both, of two different forms—coupling via time varying fields:

$$\frac{dV}{dT} C_P$$

or by injection of parasitic currents by changes in capacitance due to mechanical vibration:

$$\frac{dCp}{dT} V$$

*Teflon is a registered trademark of E.I. du Pont Co.

Both proper shielding and rigid mechanical mounting of components help minimize error currents from both of these sources.

OFFSET NULLING

The AD795's input offset voltage can be nulled (mini-DIP package only) by using balance Pins 1 and 5, as shown in Figure 34. Nulling the input offset voltage in this fashion will introduce an added input offset voltage drift component of 2.4 μV/°C per millivolt of nulled offset.

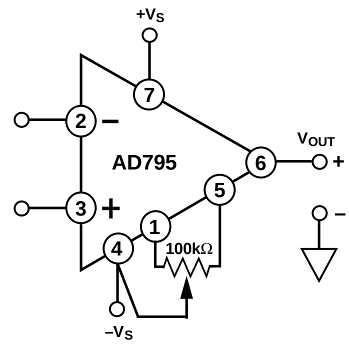


Figure 34. Standard Offset Null Circuit

The circuit in Figure 35 can be used when the amplifier is used as an inverter. This method introduces a small voltage in series with the amplifier's positive input terminal. The amplifier's input offset voltage drift with temperature is not affected. However, variation of the power supply voltages will cause offset shifts.

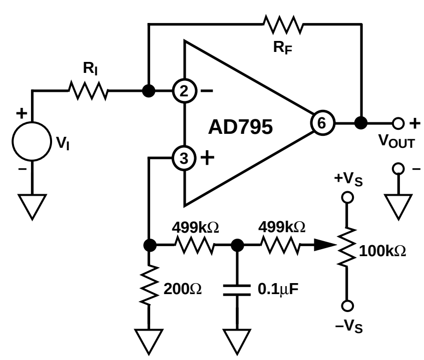


Figure 35. Alternate Offset Null Circuit for Inverter

AC RESPONSE WITH HIGH VALUE SOURCE AND FEEDBACK RESISTANCE

Source and feedback resistances greater than 100 kΩ will magnify the effect of input capacitances (stray and inherent to the AD795) on the ac behavior of the circuit. The effects of common-mode and differential input capacitances should be taken into account since the circuit's bandwidth and stability can be adversely affected.

In a follower, the source resistance, R_S, and input common-mode capacitance, C_S (including capacitance due to board and capacitance inherent to the AD795), form a pole that limits circuit bandwidth to $1/2\ \pi\ R_S C_S$. Figure 36 shows the follower pulse response from a 1 MΩ source resistance with the amplifier's input pin isolated from the board, only the effect of the AD795's input common-mode capacitance is seen.

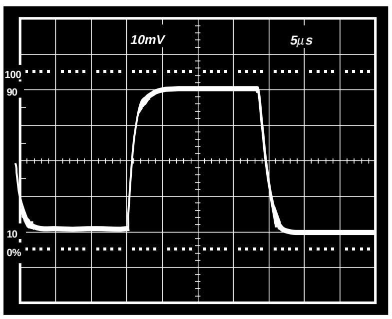


Figure 36. Follower Pulse Response from 1 MΩ Source Resistance

In an inverting configuration, the differential input capacitance forms a pole in the circuit's loop transmission. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1 MΩ, and the input pin isolated from the board appears in Figure 37. Figure 38 shows the response of the same circuit with a 1 pF feedback capacitance. Typical differential input capacitance for the AD795 is 2 pF.

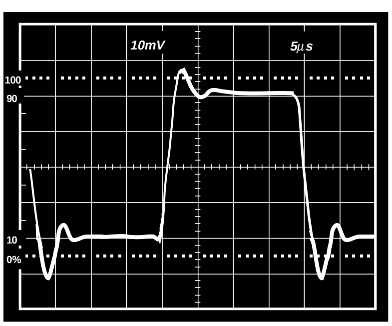


Figure 37. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

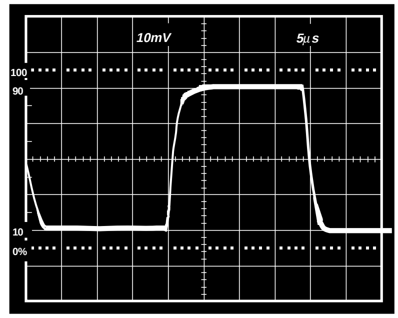


Figure 38. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1 pF Feedback Capacitance

OVERLOAD ISSUES

Driving the amplifier output beyond its linear region causes some sticking; recovery to normal operation is within 2 µs of the input voltage returning within the linear range.

If either input is driven below the negative supply, the amplifier's output will be driven high, causing a phenomenon called phase reversal. Normal operation is resumed within 30 µs of the input voltage returning within the linear range.

Figure 39 shows the AD795's input currents versus differential input voltage. Picoamp level input current is maintained for differential voltages up to several hundred millivolts. This behavior is only important if the AD795 is in an open-loop application where substantial differential voltages are produced.

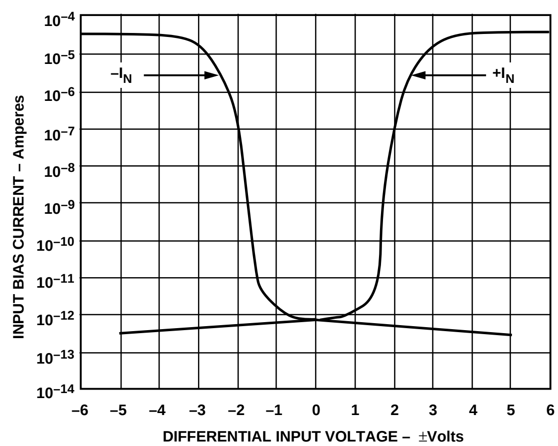


Figure 39. Input Bias Current vs. Differential Input Voltage

INPUT PROTECTION

The AD795 safely handles any input voltage within the supply voltage range. Some applications may subject the input terminals to voltages beyond the supply voltages—in these cases, the following guidelines should be used to maintain the AD795's functionality and performance.

If the inputs are driven more than a 0.5 V below the minus supply, milliamp level currents can be produced through the input terminals. That current should be limited to 10 mA for "transient" overloads (less than 1 second) and 1 mA for continuous overloads, this can be accomplished with a protection resistor in the input terminal (as shown in Figures 40 and 41). The protection resistor's Johnson noise will add to the amplifier's input voltage noise and impact the frequency response.

Driving the input terminals above the positive supply will cause the input current to increase and limit at 40 µA. This condition is maintained until 15 volts above the positive supply—any input voltage within this range does not harm the amplifier. Input voltage above this range causes destructive breakdown and should be avoided.

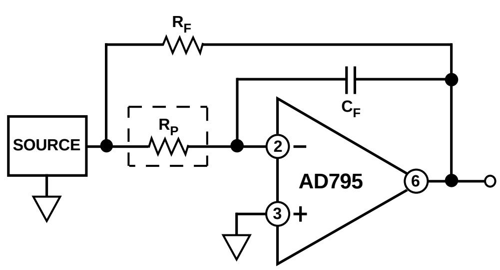


Figure 40. Inverter with Input Current Limit

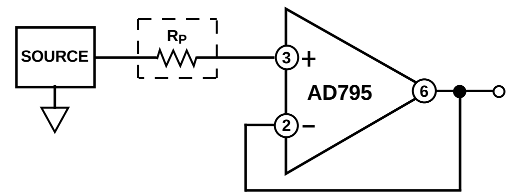


Figure 41. Follower with Input Current Limit

Figure 42 is a schematic of the AD795 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Low leakage diodes (less than 1 pA), such as the FD333s should be used, and should be shielded from light to keep photocurrents from being generated. Even with these precautions, the diodes will measurably increase the input current and capacitance.

In order to achieve the low input bias currents of the AD795, it is not possible to use the same on-chip protection as used in other Analog Devices op amps. This makes the AD795 sensitive to handling and precautions should be taken to minimize ESD exposure whenever possible.

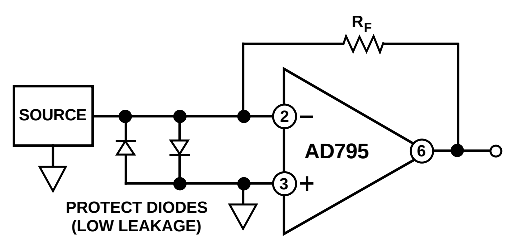


Figure 42. Input Voltage Clamp with Diodes

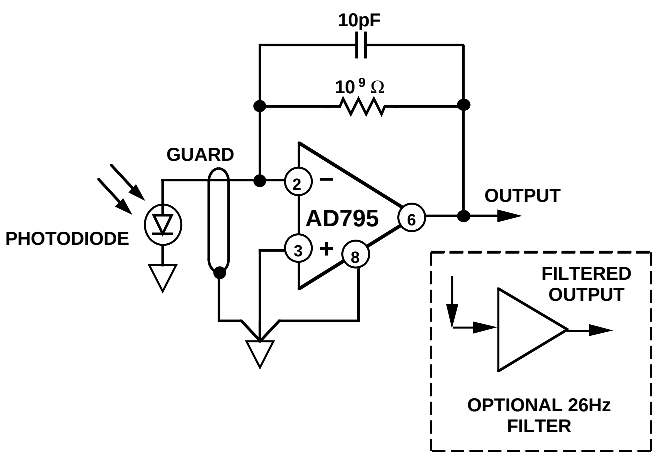


Figure 43. The AD795 Used as a Photodiode Preamplifier

Preamplifier Applications

The low input current and offset voltage levels of the AD795 together with its low voltage noise make this amplifier an excellent choice for preamplifiers used in sensitive photodiode applications. In a typical preamp circuit, shown in Figure 43, the output of the amplifier is equal to:

$$V_{OUT} = I_D\,(Rf) = Rp\,(P)\,Rf$$

where:

I_D = photodiode signal current (Amps)

Rp = photodiode sensitivity (Amp/Watt)

Rf = the value of the feedback resistor, in ohms.

P = light power incident to photodiode surface, in watts.

An equivalent model for a photodiode and its dc error sources is shown in Figure 44. The amplifier's input current, I_B, will contribute an output voltage error which will be proportional to the value of the feedback resistor. The offset voltage error, V_{OS}, will cause a "dark" current error due to the photodiode's finite shunt resistance, Rd. The resulting output voltage error, V_E, is equal to:

$$V_E = (1 + Rf/Rd)\,V_{OS} + Rf\,I_B$$

A shunt resistance on the order of 10^9 ohms is typical for a small photodiode. Resistance Rd is a junction resistance which

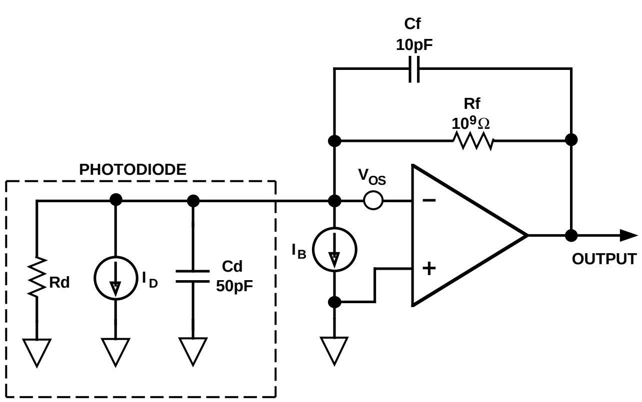


Figure 44. A Photodiode Model Showing DC Error Sources

will typically drop by a factor of two for every 10°C rise in temperature. In the AD795, both the offset voltage and drift are low, this helps minimize these errors.

Minimizing Noise Contributions

The noise level limits the resolution obtainable from any preamplifier. The total output voltage noise divided by the feedback resistance of the op amp defines the minimum detectable signal current. The minimum detectable current divided by the photodiode sensitivity is the minimum detectable light power.

Sources of noise in a typical preamp are shown in Figure 45. The total noise contribution is defined as:

$$\overline{V_{OUT}} = \sqrt{(\overline{in}^2 + \overline{if}^2 + \overline{is}^2)\left(\frac{Rf}{1+s\,(Cf)\,Rf}\right)^2 + (\overline{en}^2)\left(1+\frac{Rf}{Rd}\left(\frac{1+s\,(Cd)\,Rd}{1+s\,(Cf)\,Rf}\right)\right)^2}$$

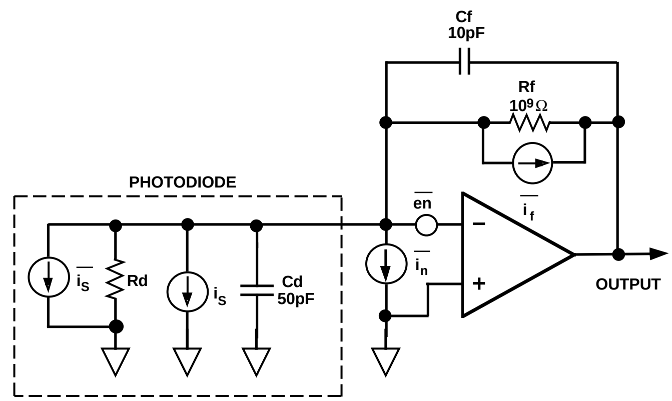


Figure 45. Noise Contributions of Various Sources

Figure 46, a spectral density versus frequency plot of each source's noise contribution, shows that the bandwidth of the amplifier's input voltage noise contribution is much greater than its signal bandwidth. In addition, capacitance at the summing junction results in a "peaking" of noise gain in this configuration. This effect can be substantial when large photodiodes with large shunt capacitances are used. Capacitor Cf sets the signal bandwidth and also limits the peak in the noise gain. Each source's rms or root-sum-square contribution to noise is obtained by integrating the sum of the squares of all the noise sources and then by obtaining the square root of this sum. Minimizing the total area under these curves will optimize the preamplifier's overall noise performance.

An output filter with a passband close to that of the signal can greatly improve the preamplifier's signal to noise ratio. The photodiode preamplifier shown in Figure 45—without a bandpass filter—has a total output noise of 50 µV rms. Using a 26 Hz single pole output filter, the total output noise drops to 23 µV rms, a factor of 2 improvement with no loss in signal bandwidth.

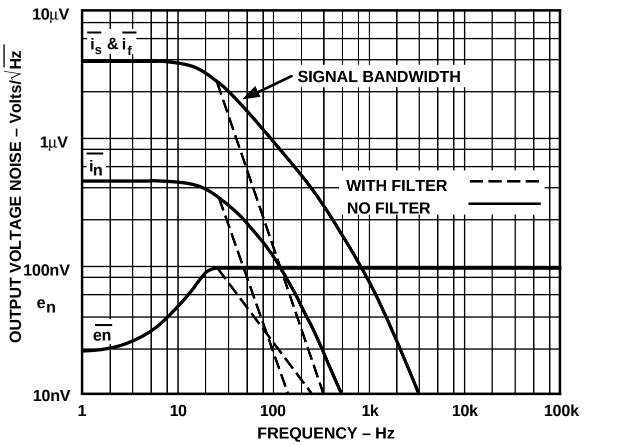


Figure 46. Voltage Noise Spectral Density of the Circuit of Figure 45 With and Without an Output Filter

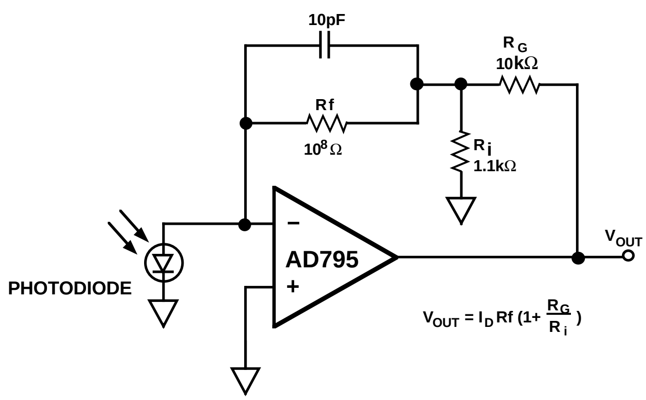


Figure 47. A Photodiode Preamp Employing a "T" Network for Added Gain

Using a "T" Network

A "T" network, shown in Figure 47, can be used to boost the effective transimpedance of an I-to-V converter, for a given feedback resistor value. However, amplifier noise and offset voltage contributions are also amplified by the "T" network gain. A low noise, low offset voltage amplifier, such as the AD795, is needed for this type of application.

A pH Probe Buffer Amplifier

A typical pH probe requires a buffer amplifier to isolate its 10^6 to 10^9 Ω source resistance from external circuitry. Just such an amplifier is shown in Figure 48. The low input current of the AD795 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50 mV per pH unit at room temperature, has a +3300 ppm/°C temperature coefficient. The buffer of Figure 48 provides an output voltage equal to 1 volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor, part number Q81, 1 kΩ, 1%, +3500 ppm/°C, available from Tel Labs Inc.

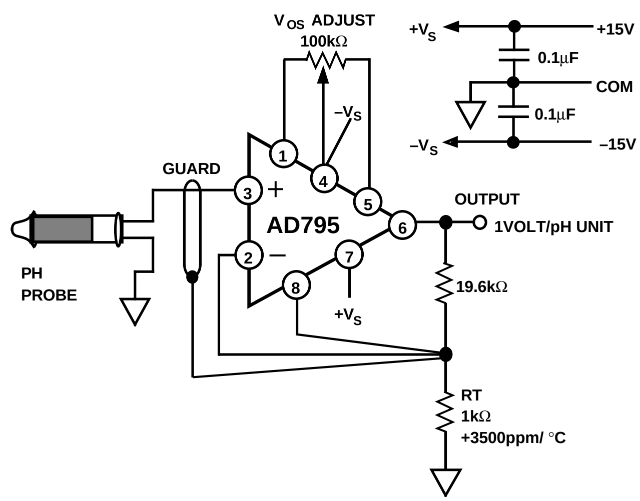
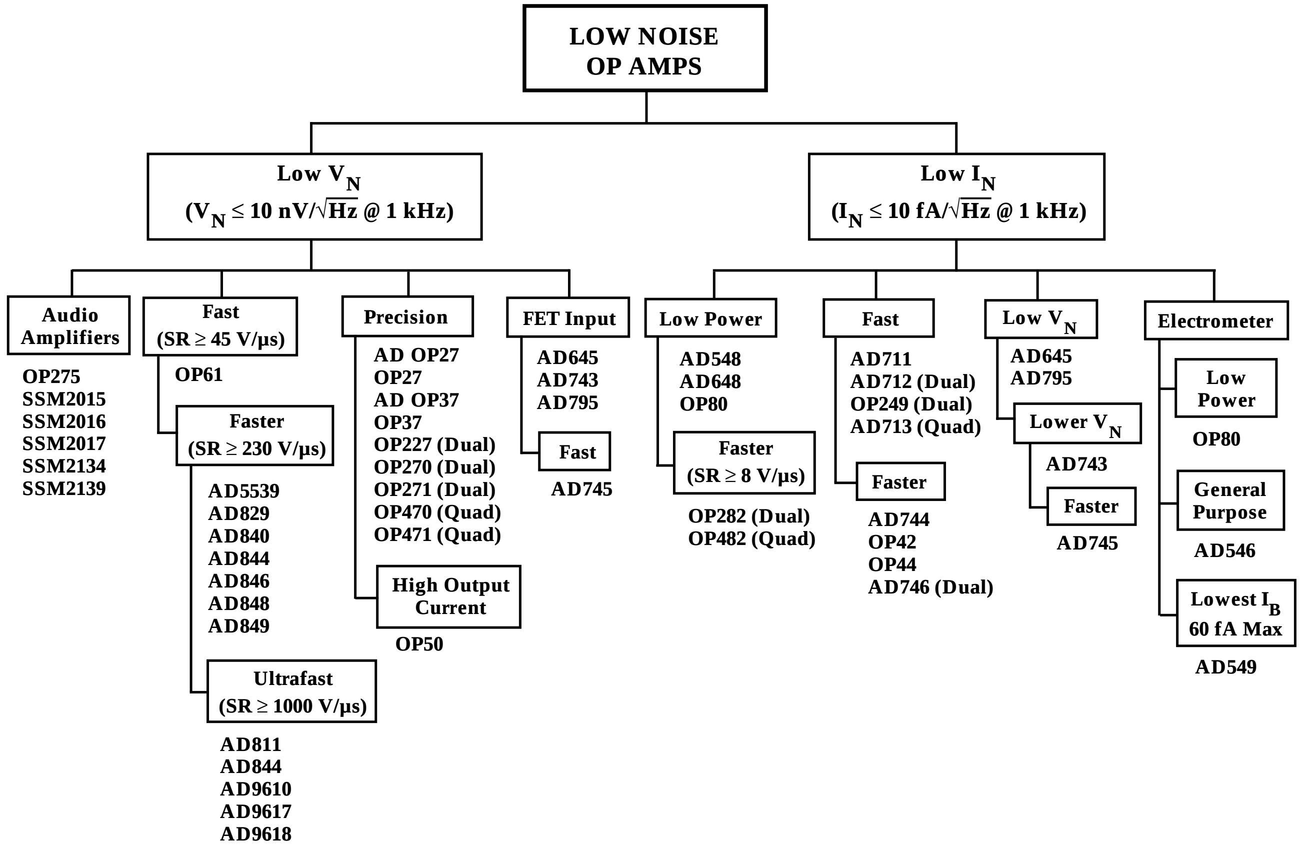


Figure 48. A pH Probe Amplifier

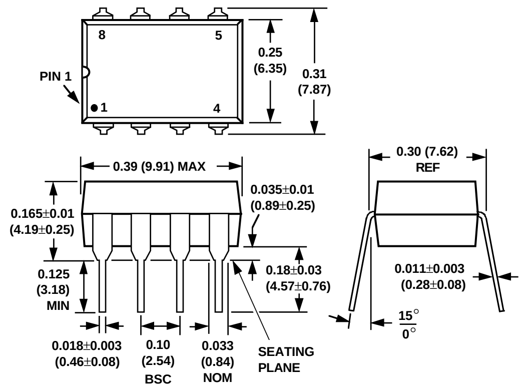


Low Noise Op Amp Selection Tree

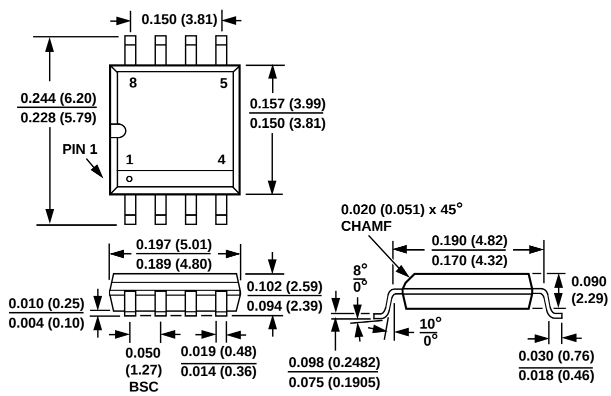
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic Mini-DIP (N) Package



8-Pin SOIC (R) Package



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